SYMMETRIC HEMT DRAIN CURRENT MODEL FOR INTERMODULATION DISTORTION PREDICTION

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ABSTRACT

A new large-signal HEMT drain current model is presented that accurately describes not only the AC gain and resistance of the device, but also their derivatives with respect to bias. This allows the accurate simulation of linear and nonlinear performance over bias. The model is scalable, and is shown to predict S-parameters, power compression characteristics and intermodulation distortion of devices and circuits over a range of frequencies, biases and device sizes.

INTRODUCTION

In this work, a large-signal explicit HEMT model has been developed for small-signal applications. Compared to small-signal nonlinear models, such as a Volterra series [1], a large-signal description has potentially superior performance at higher power levels. The descriptions can be scalable and also have applicability to bias and conditions outside the range of measurements used to fit model parameters.

To be applicable to small-signal simulations, the transistor model needs to fit the high-order differential behaviour of the device. Thus the mathematic expressions used need to be continuous and smooth. Good small-signal performance can be obtained when the parameters are fitted to nonlinear measurements.

This paper describes the nonlinear drain current model, then an example of fitting the drain current model to measurements is given. The performance of the model in predicting S-parameters up to 50 GHz and nonlinear power compression measurements for different device sizes and biases are discussed.

DRAIN CURRENT MODEL

The drain current model is implemented by a continuous function that is symmetric with respect to gate-source and gate-drain potentials. The implementation uses two opposing currents to give a total drain-source current as follows.

$$i_D = \beta \left[F(v_{GS}, v_{GD}) - F(v_{GD}, v_{GS}) \right] (1 - \delta P) \tag{1}$$

where β is the transconducatance parameter, v_{GS} is the gate-source potential, v_{GD} is the gate-drain potential, δ is the self-heating derating due to power dissipation P, and F is a power-law of transformed potentials given by

$$F(x, y) = U(V(x, y), V(y, x))^{Q(x,y)} \tag{2}$$

where

$$U(x,y) = \frac{1}{2}\left(x + \frac{y^2}{\xi + y} + \sqrt{\left(x - \frac{y^2}{\xi + y}\right)^2 + Z^2}\right) \tag{3}$$

and

$$V(x,y) = \sigma \ln\left(\exp\left(\frac{x - \gamma y - V_{TO}}{\sigma}\right) + 1\right) \tag{4}$$

and ξ, σ, γ, and V_{TO} are fitting parameters respectively related to the velocity saturation potential, rate of transition to subthreshold conduction, the intrinsic gain, and the pinch-off potential of the transistor.

The transformation (4), which is the core of PS MESFET model [2], gives the potential above pinch-off x modulated by y. It is an infinitely differentiable function that well describes the derivative behaviour of FETs. In the saturated operating mode where $v_{GS} < v_{GD}$, $V(v_{GS}, v_{GD}) \approx v_{GS} - V_{TO}$ and $V(v_{GD}, v_{GS}) \approx 0$.

The base function (3) limits the minimum value of x to $y\xi/(\xi + y)$, which implements early current saturation due to electron velocity saturation [2]. If pinch-off saturation occurs ($\xi \to \infty$), then the second term (1) goes to zero, whereas for low ξ, (3) becomes a non-zero constant at a lower saturation potential. The rate of transition into saturation is set by Z.

The power Q is given by

$$Q(x,y) = Q(y,x) = \frac{Q_O}{1 + Q_G\left(V(x,y) + V(y,x) + \sqrt{(V(x,y) - V(y,x))^2 + Z^2}\right) + Q_D(x-y)^2} \tag{5}$$

where Q_G sets the rate at which transconductance reduces as the device turns on and Q_D sets a dependence on drain-source potential. For a MESFET, these parameters are zero, whereas for a HEMT, they are used to implement transconductance peaking [3].

The power, P, is the instantaneous power convolved with the thermal impulse response of the transistor. In the frequency domain, this is implemented by

$$P(\omega) = \frac{(v_{GS} - v_{GD})i_D}{(1 + j\omega/\omega_o)^n} \tag{6}$$

where ω_o is related to the time constant of heating and n is the order of the thermal response, which is less than unity [4].

This model is capable of fitting high-order differential characteristics of HEMTs and MESFETs. Its symmetry guarantees continuity near $v_{DS} = 0$. The smooth transition to the pinch-off and saturated regions (implemented through nested transformations [5]) provides sensible derivative behaviour. Thus, the model has been designed to predict small-signal nonlinearity accurately.

CURRENT MODEL FITTING

Traditionally, large-signal device models are fitted to dc and S-parameter data at a range of biases. However, to correctly model distortion behavior, it is necessary to ensure that the derivatives of the drain current with respect to bias are accurately modelled and fitted [6]. There are a number of methods to measure these derivatives. They can be found using pulsed bias measurements [7], distortion measurements [8], load pull measurements [9] or S-parameter measurements [10]. S-parameter measurements are used here for a number of reasons. The S-parameters can be measured at frequencies much higher than any device dispersion effects [11], they include phase information, and are required for the fitting of the other elements in the FET equivalent circuit model anyway (see the next section).

The small-signal transconductance (G_m) and drain conductance (G_d) of the FET are measured using S-parameters, as explained in the next section. They are measured over a fine grid of biases, gate voltages from -1 to 0 V in 0.05 V steps, and drain voltages from 0 to 5 V in 0.25 V steps. The derivatives of G_m and G_d with respect to bias specifies the nonlinearity of the drain current. The drain current of a FET can be represented as a 2-dimensional Taylor series,

with gate voltage and drain voltage being the controlling variables.

$$\begin{aligned} i_D &= I_D + \frac{\partial i_D}{\partial v_G} v_g + \frac{\partial i_D}{\partial v_D} v_d + \frac{1}{2}\Big(\frac{\partial^2 i_D}{\partial v_G^2} v_g^2 + 2\frac{\partial^2 i_D}{\partial v_G \partial v_D} v_g v_d + \frac{\partial^2 i_D}{\partial v_D^2} v_d^2\Big) \\ &\quad + \frac{1}{6}\Big(\frac{\partial^3 i_D}{\partial v_G^3} v_g^3 + 3\frac{\partial^3 i_D}{\partial v_G^2 \partial v_D} v_g^2 v_d + 3\frac{\partial^3 i_D}{\partial v_G \partial v_D^2} v_g v_d^2 + \frac{\partial^3 i_D}{\partial v_D^3} v_d^3\Big) + \ldots \qquad (7) \\ &= I_D + G_m v_g + G_d v_d + G_{m2} v_g^2 + G_{md} v_g v_d + G_{d2} v_d^2 + G_{m3} v_g^3 + G_{m2d} v_g^2 v_d + G_{md2} v_g v_d^2 + G_{d3} v_d^3 + \ldots \qquad (8) \end{aligned}$$

The large signal drain current is $i_D = I_D + i_d$, the sum of the DC and AC components. Similar notation is used for the gate voltage v_G and drain voltage v_D. The DC components and derivatives are evaluated at a particular bias, ie $I_D = I_D(V_G, V_D)$. The small signal AC voltages v_g and v_d represent the voltage swing around the quiescent bias. The equations (7-8) have been shown up to the third-order, but they can be expanded up to any order. However, measurement noise is exacerbated by differentiation, so this limits the order of the Taylor series that can be extracted in practice.

From the equivalent circuit extraction, the first-order transconductance (G_m) and drain conductance (G_d) in (8) are known. Then, the higher-order coefficients can be found by taking the derivatives of these parameters with respect to bias, with reference to (7). For example,

$$G_{m2} = \frac{1}{2}\frac{\partial G_m}{\partial v_G} \qquad (9)$$

and

$$G_{md2} = \frac{1}{2}\frac{\partial G_d}{\partial v_G \partial v_D}. \qquad (10)$$

These derivatives can be computed using standard numerical methods. For example, at a bias (V_G, V_D),

$$G_{m2}(V_G, V_D) = \frac{1}{2}\frac{\partial G_m}{\partial v_G}\Big|_{v_G=V_G, v_D=V_D} = \frac{1}{2}\frac{G_m(V_G + h, V_D) - G_m(V_G, V_D)}{h}. \qquad (11)$$

The parameter h in (11) is set to the bias grid spacing of that variable. For example, in our case, the grid spacing for V_G was 0.05 V. Similar equations can be found to evaluate all the other coefficients.

Following this procedure, each coefficient in (8) is known over a grid of V_G and V_D. For example, G_{md} of a 4 finger by 100μm pHEMT is shown in Fig. 1.

These measurements can then be used to fit the drain current model in a simulator. The model parameters are adjusted to accurately fit the measured drain current derivatives over both V_G and V_D. Fig. 2 shows the modelled and measured coefficients along $V_D = 4$ V after fitting. The model fits the measurements well over the range of drain biases typically used in amplifier applications. In Fig. 2(c), the coefficients G_{d2}, G_{md2} and G_{d3} seem to not be fitted well. However, these coefficients are very small, and difficult to measure. In addition, their contribution to the overall distortion is small. The fitting of the important coefficients over bias is very good. Therefore, we would expect the model to simulate intermodulation distortion very well, provided that the other elements in the FET equivalent circuit, Fig. 3, are modelled accurately.

OTHER MODEL ELEMENTS AND S-PARAMETER PREDICTION

A HEMT, operating at high frequencies, can be represented by the equivalent circuit in Fig. 3. The elements outside the dotted rectangle are the extrinsic access parasitics, and can be considered constant with bias. Inside the rectangle are the intrinsic elements, which change with bias and thus are nonlinear. At each bias of interest, the linear part of each of the components in Fig. 3 can be found by measuring the S-parameters of the device at each bias of interest, and then using a method such as the widely accepted one proposed by Dambrine [12] to extract the component values from the S-parameters. At this point, we have the linear equivalent circuit model at a range of biases.

The large-signal model currently uses the nonlinear drain current described above. The remaining intrinsic elements in Fig. 3 are implemented as look-up tables, referenced by V_G and V_D. The elements are scalable, that is, they will automatically be updated in the simulator with a change in the device size. Standard scaling rules were used, similar to those in [13]. For example, the drain current scales linearly with device size.

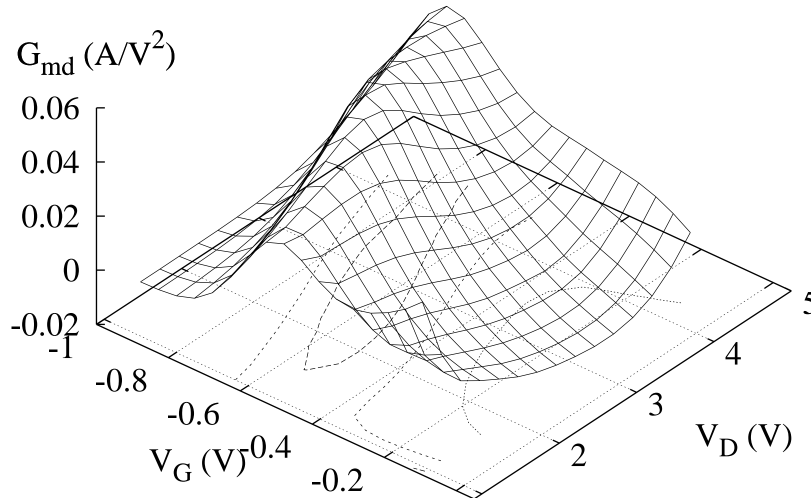

Fig. 1. Measured G_{md} of a 4 finger by 100μm pHEMT.

The S-parameter fit at two representative biases and device sizes are shown in Figs. 4-5. The S-parameter fit up to 50 GHz is good for different device sizes and biases. This gives confidence in the equivalent circuit extraction and large signal drain current model.

COMPRESSION VERIFICATION

To verify the nonlinear prediction capability of the model, power compression characteristics were measured for a range of device sizes, biases and frequencies. The single-tone sinusoidal input power was swept from well backed off (when the device is operating nearly linearly), to beyond the 1dB compression point. The harmonics from the signal generator were carefully filtered, to ensure that a pure sinusoid was exciting the device. The fundamental and harmonics were measured at the device output by a spectrum analyser.

Two representative comparisons are shown in Figs. 6-7 below. The first one is of a small device, with the fundamental at 45 MHz. The simulation of both the fundamental compression characteristics, and the harmonics (at 90 MHz and 135 MHz) is very accurate.

In Fig. 7, measurements of a larger device with the fundamental frequency increased to 13 GHz are shown. Thus, the harmonics are at 26 GHz and 39 GHz. Once again, the fundamental compression characteristic is predicted very accurately by the model. The harmonics at higher power levels are also predicted well. At lower power levels, the harmonic prediction is not as good. This is most probably due to nonlinearities in the device that only become significant at higher frequencies, such as the nonlinear gate-source capacitance. At this stage, all intrinsic capacitors are modelled by linear components, with values coming from a look-up table. Work on a nonlinear charge model is currently being undertaken, which will improve the harmonic predictions at higher frequencies.

INTERMODULATION DISTORTION SIMULATION

To verify the intermodulation distortion prediction capability of the model, a MMIC amplifier was measured. It is a two-stage 15GHz amplifier, using 2 pHEMTs. The input signal was the combined outputs of two signal generators, giving

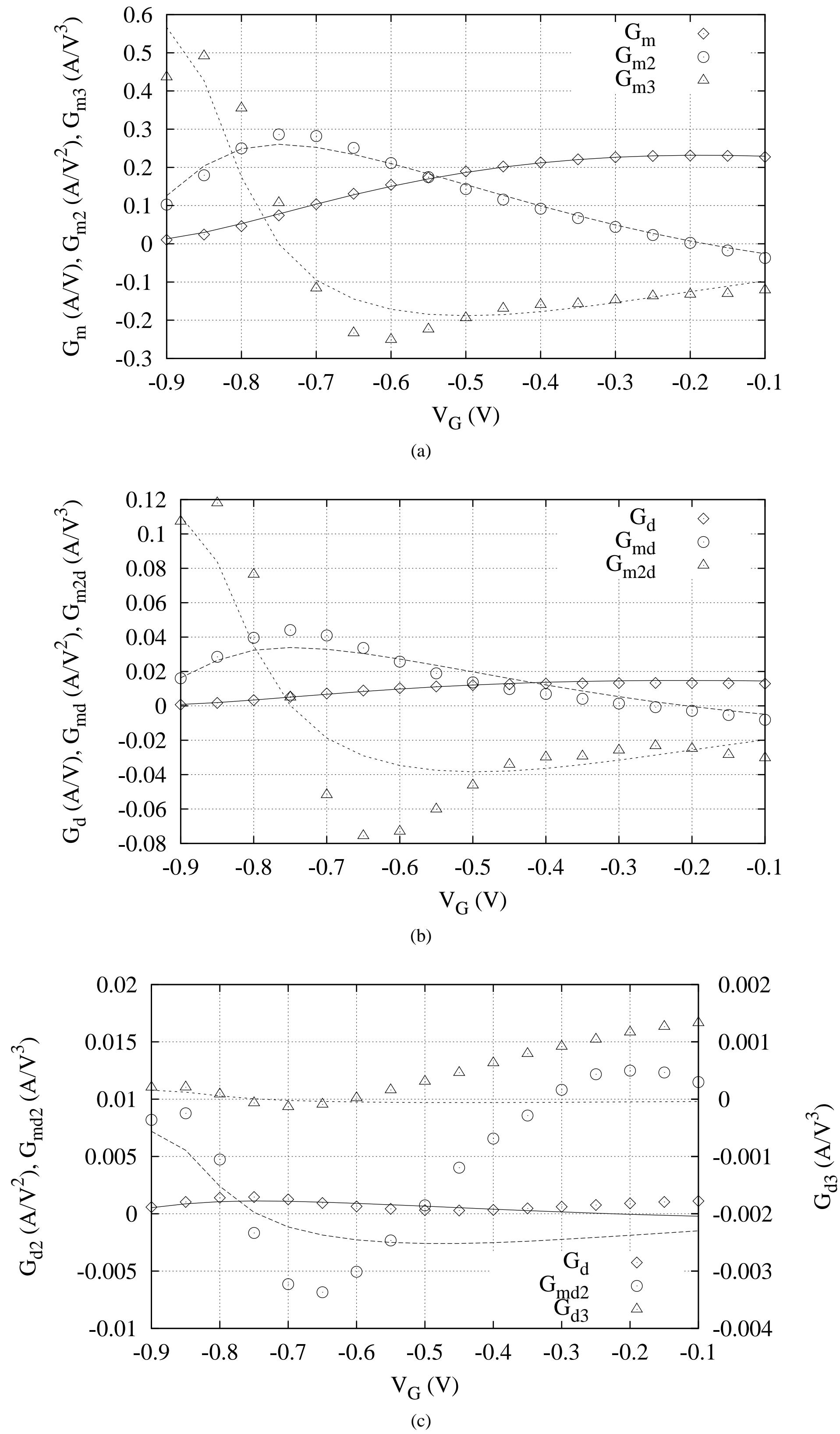

Fig. 2. Modelled and measured drain current derivatives of the 4 finger by 100μm pHEMT at $V_D = 4$ V.

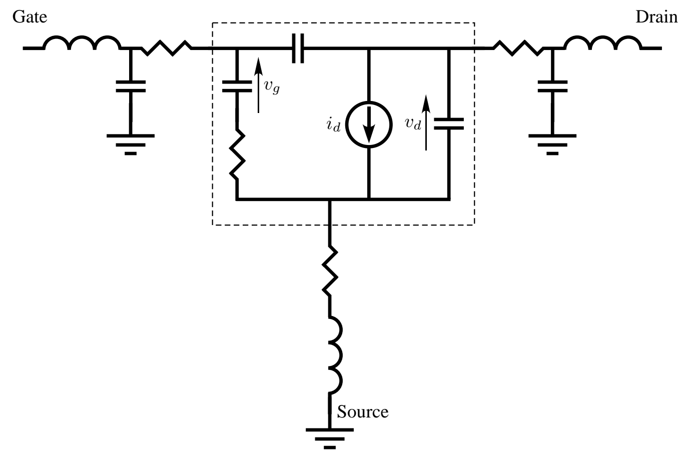

Fig. 3. FET equivalent circuit.

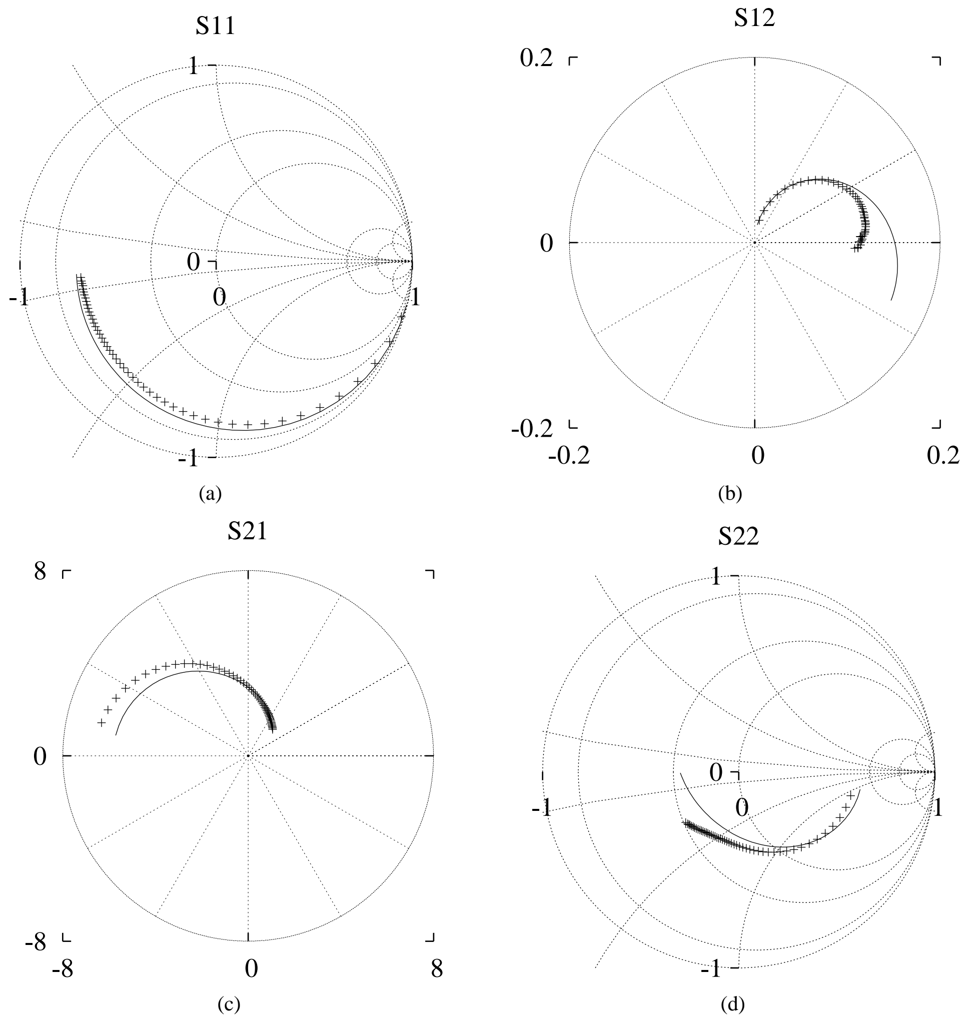

Fig. 4. Measured and modelled S-parameters of the 2 finger by 75μm pHEMT at $V_D = 2$ V and $V_G = -0.1$ V from 2 GHz to 50 GHz.

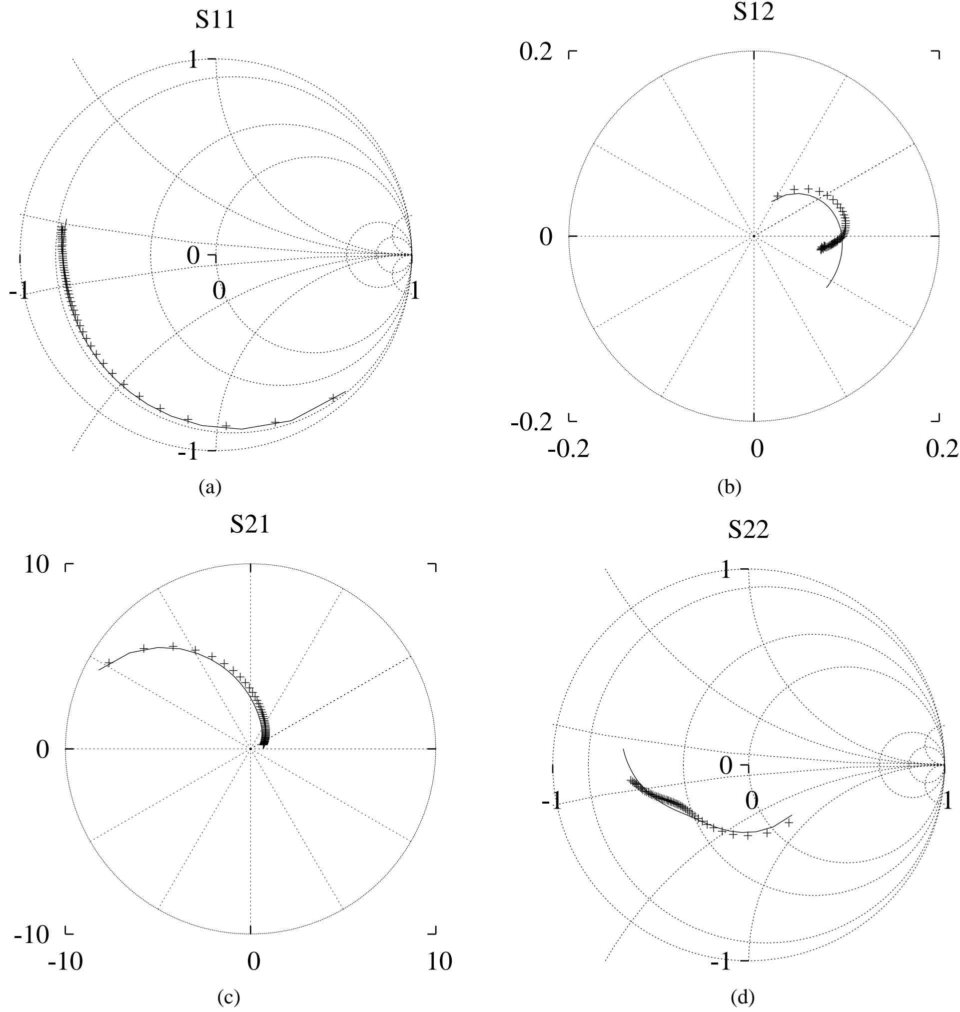

Fig. 5. Measured and modelled S-parameters of the 4 finger by 100μm pHEMT at $V_D = 4$ V and $V_G = -0.5$ V from 2 GHz to 50 GHz.

two tones near 15 GHz with 100 MHz tone spacing. The output of the amplifier was measured with a spectrum analyser. The simulated and measured intermodulation distortion is shown in Fig. 8. These are good results for intermodulation distortion prediction at a high frequency. The discrepancy at higher gate biases is most likely due to charge trapping effects that have not yet been implemented in the large-signal model [14]. This agreement gives confidence in the drain current model formulation, because it can accurately predict small-signal intermodulation distortion at a range of biases.

CONCLUSION

A new symmetric HEMT drain current model has been presented. It has been shown to describe the derivatives of the drain current accurately, over a range of biases and device sizes. This leads to good linear S-parameter and nonlinear compression predictions. In addition, the measured and simulated intermodulation distortion of a 15GHz MMIC amplifier were compared, showing the capability of the model to accurately predict intermodulation distortion.

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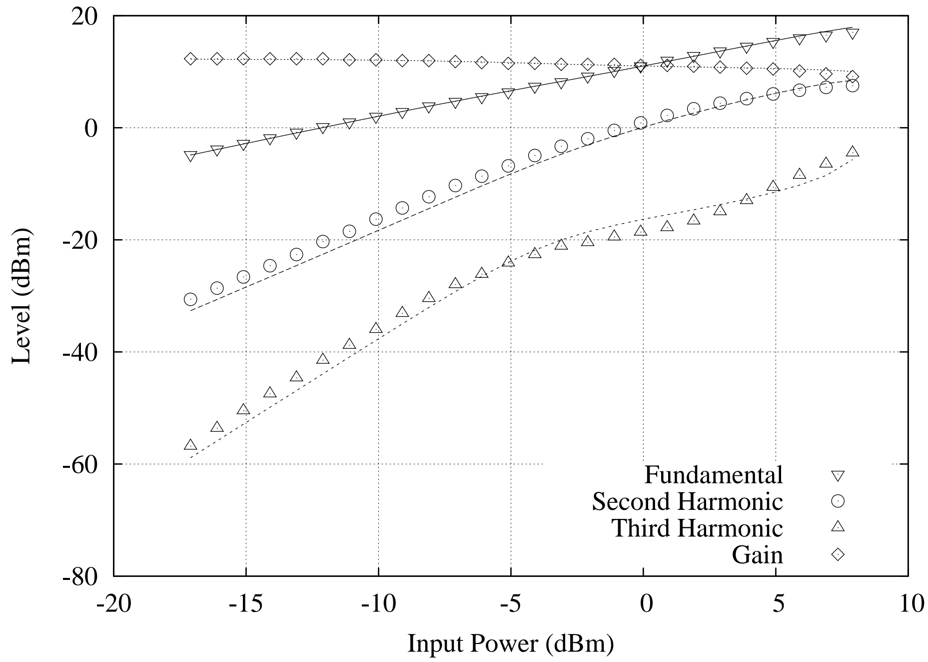

Fig. 6. Measured (points) and simulated (lines) power compression characteristics of a 2 finger by 75μm pHEMT. The fundamental frequency is 45 MHz, and the bias is $V_D = 4$ V, $V_G = -0.6$ V.

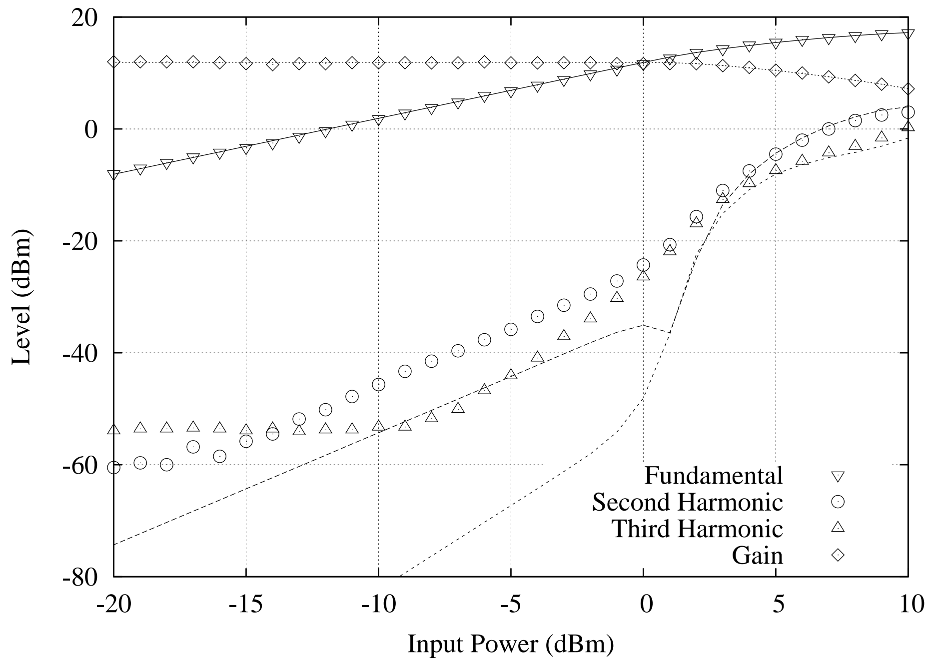

Fig. 7. Measured (points) and simulated(lines) power compression characteristics of a 4 finger by 100μm pHEMT. The fundamental frequency is 13 GHz, and the bias is $V_D = 2$ V, $V_G = -0.1$ V.

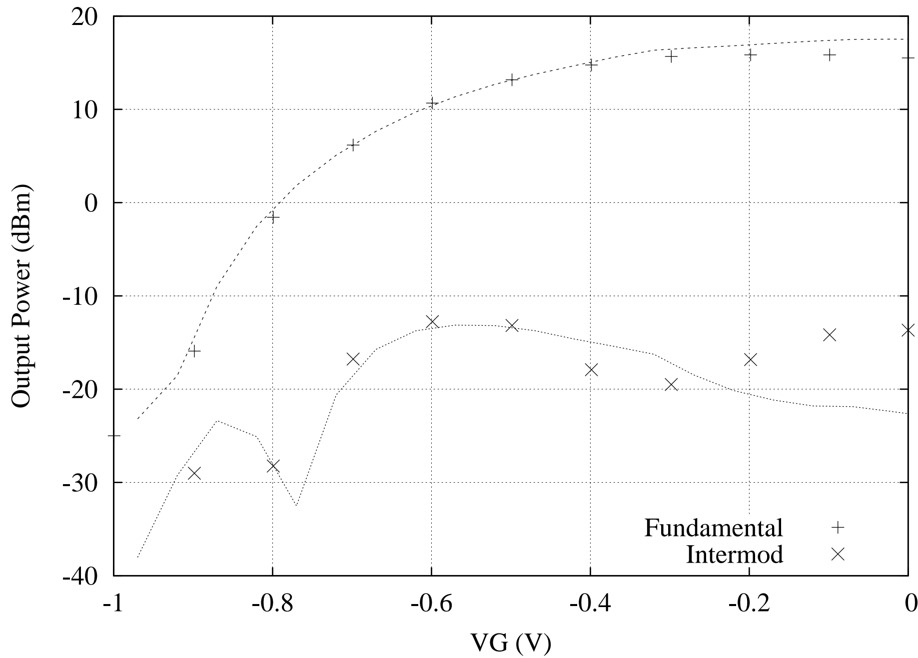

Fig. 8. Measured (points) and simulated (lines) intermodulation distortion of a 15GHz two-stage MMIC amplifier using two 4 finger by 100μm pHEMTs. The tone spacing is 100 MHz, and the drain bias is 4 V.

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